WEST VIRGINIA UNIVERSITY

COLLEGE OF ENGINEERING AND MINERAL RESOURCES

THE LANE DEPARTMENT OF COMPUTER SCIENCE AND ELECTRICAL ENGINEERING

Course Syllabus

CpE 442/ CS 455

INTRODUCTION TO COMPUTER ARCHITECTURE

Instructor: Hany H. Ammar, Professor of Computer Engineering, Office: 739 Engineering Sc. Buildg, Evansdale Campus, WVU, Morgantown, WV 26506, Ph: 293-9682, Fax 293-8602, E-mail address:hammar@wvu.edu

Office Hours: Tuesdays: 10:30 -11:45 am, Wednesdays 10:30 am – 12:00 noon, Thursdays 10:00 – 11:00 am

Prerequisites: Math 375, CPE 310, and CPE 311/ or CS 350

Text: Computer Organization and Design: The Hardware/Software Interface, **3rd Ed.**, D. A. Patterson and J. L. Hennessy, Morgan Kaufmann Publishers. 2007

References:

1. Structured Computer Organization, A. S. Tanenbaum, Prentice-Hall.

2. Computer Hardware/Software Architecture, W. Toy and B. Zee, Prentice-Hall.

3. Modern Computer Architecture, Mohammed Rafiguzzaman and R. Chandra, West Publishing Company.

4. Computer Organization, 5th ed, C. Hamacher, Z. Varbesic, S. Zaky, McGrawHill.

COURSE OBJECTIVES:

Students should be able to do the following:

- Relate performance metrics to architectural parameters.
- Specify the important tradeoffs in instruction set design.
- Identify the problems and tradeoffs encountered in the design of computer processors, and specify specific example from the current state of the art family of Reduced Instruction Set Architectures (the MIPS architecture).
- Relate the concept of memory hierarchy to cache designs and the design of virtual memory management units.
- Identify the problems encountered in I/O subsystem design, and relate such problems to the design of processor and memory subsystems, and identify new technologies for disks and tapes.
- Identify the main features of parallel architectures in terms of interconnection networks and the extended concepts of instruction set parallelism

Topics: **#weeks**

- Overview of Computer Architecture Ch. 1, 1.1-1.3, 1.5-1.6 1/2

- The Role of Performance, Ch. 4, 4.1-4.6 ***HW1*** 1

- Instruction Set Design Tradeoffs, Ch. 2, 2.1-2.8 1

- The MIPS Instruction Set Architecture Ch. 2, 2.9-2.15

HW2 :Text problems
2.29,2.34,2.49,2.51 1

- The Processor Data Path and Control 3

The Single Cycle Data Path Ch. 5, 5.1-5.3 (Ch. 5 Text Figures)

The Single Cycle Control Ch. 5, 5.4 ***HW3*** **5.8, 5.10, 5.13, 5.28**

The Multi Cycle Data Path Ch. 5, 5.5

The Multi Cycle Control, Ch. 5, 5.5 (Ch. 5 More Text Figures) ***Hw4:***

5.32, 5.34

Microprogramming and Exceptions Ch. 5, 5.6-5.7 Appendix C

- Pipelining Architecture Ch. 6, 6.1 - 6.6 2

Design of a Pipeline Processor

Design of a Pipeline Processor ***hw5: 6.4, 6.17, 6.18, 6.22***

- The Memory Hierarchy, Ch. 7, 7.1-7.5 2

The Memory Subsystem

Cache Design

Virtual Memory ***hw6:7.12, 7.14, 7.46, 7.52***

- **I/O Characteristics and Performance,** Ch. 8, 8.1-8.4 1

  The I/O Subsystem

  Bus Architectures

- **Introduction to Parallel Architectures,** Ch. 9. 9.1, 9.4 1/2

  Interconnection Networks

  Instruction Level Parallelism

- **Review for the term exam**

-**Project Presentations: Last Week of Classes, See Term Project Assignment**

Grading:

Attendance	5%
Homework	35%
Project	35% here is an example previous presentation and report

Project Presentations held during the last 2 weeks of classes

Project Report due Thursday of Finals Week

Term Examination 25%, Tentative Date: in Class Exam. Thursday November 20, 2014.

The project involves a comprehensive study of the current processor architectures (such as the Alpha architecture, the Intel IA 64 architecture, etc.). Overview of architecture and how it briefly compares to others and details of some of its main features should be thoroughly researched. The projects will be conducted by groups of 2 or 3 students. A final report and an in-class presentation are required. The report should contain a section on the contributions of each member of the group, and each member should take part in the project presentation.