Course Syllabus
CpE 442/ CS 455
INTRODUCTION TO COMPUTER ARCHITECTURE

Instructor: Hany H. Ammar, Professor of Computer Engineering, Office: 739 Engineering Sc. Buildg, Evansdale Campus, WVU, Morgantown, WV 26506, Ph: 293-9682, Fax 293-8602, E-mail address: hammar@wvu.edu
Office Hours: Mondays-Wednesdays 10:30 am -12:00 pm

Prerequisites: Math 375, CPE 310, and CPE 311/ or CS 350


References:

COURSE OBJECTIVES:
- Students should be able to do the following:
  - Identify the levels of abstractions and the levels of organization in computer architecture design
  - Relate performance metrics to architectural parameters.
  - Specify the important tradeoffs in instruction set design.
Identify the problems and tradeoffs encountered in the design of computer processors, and specify specific examples from the current state of the art family of Reduced Instruction Set Architectures (the MIPS architecture).

Relate the concept of memory hierarchy to cache designs and the design of virtual memory management units.

Identify the problems encountered in I/O subsystem design, and relate such problems to the design of processor and memory subsystems, and identify new technologies for disks and tapes.

Identify the main features of parallel architectures in terms of interconnection networks and the extended concepts of instruction set parallelism.

Topics:

- **Overview of Computer Architecture**  Reading Assignment: Text, Chapter 1  1/2
- **The Role of Performance**  Reading Assignment: Text, Chapter 4  HW1  1
- **Instruction Set Design Tradeoffs**  Reading Assignment: Text, Chapter 2 (Sections 2.1–2.7)  1
- **The MIPS Instruction Set Architecture**  Reading Assignment: Text, Chapter 2 (Section 2.9)  HW2: Text problems 2.29,2.34,2.49,2.51  1

- **The Processor Data Path and Control**  3
  - The Single Cycle Data Path  Reading Assignment: Text, Chapter 5 (Sections 5.1–5.4) (Ch. 5 Text Figures)  HW3 5.8, 5.10, 5.13, 5.28
  - The Single Cycle Control  5.32, 5.34
  - The Multi Cycle Data Path  Reading Assignment: Text, Chapter 5 (Sections 5.5)
  - The Multi Cycle Control (Ch. 5 More Text Figures)  Hw4
Microprogramming and Exceptions Reading Assignment: Text, Chapter 5 (Sections 5.6–5.7)

- Pipelining
  Architecture

  Design of a Pipeline Processor Reading Assignment: Text, Chapter 6 (Sections 6.1–6.6, 6.8) Design of a Pipeline Processor

  hw5: 6.4, 6.17, 6.18, 6.22

- The Memory
  Hierarchy

  The Memory Subsystem Reading Assignment: Text, Chapter 7 (Sections 7.1–7.5) Lecture Replay10

  Cache Design Lecture Replay11

  Virtual Memory Lecture Replay12

  hw6: 7.14, 7.46, 7.52

- I/O Characteristics and Performance Reading Assignment: Text, Chapter 8 (Sections 8.1–8.4)

  The I/O Subsystem

  Bus Architectures

- Introduction to Parallel Architectures

  Interconnection Networks

  Instruction Level Parallelism

- Review for the term exam

  1/2

- Project Presentations: Last Week of Classes, See Term Project Assignment

  2

Grading:

  Attendance 5%
  Homework 35%
  Project 25%

  presentation and report

  here is an example previous Project Presentations held

  during the last 2 weeks of classes

  Project Report due

  Thursday of Finals Week

  Term Examination 35%,

  Tentative Date: Wednesday November 14, 2012, an in Class Exam.

  Homework Assignments and project report submission will be
through the course link on https://ecampus.wvu.edu/. The project involves a comprehensive study of current processor architecture. An overview of the architecture and how it briefly compares to others and details of some of its main features should be thoroughly researched. The projects will be conducted by groups of 3 students. A final report and an in-class presentation are required. The report should contain a section on the contributions of each member of the group, and each member should take part in the project presentation.