West Virginia University
Statler College of Engineering and Mineral Resources
Lane Department of Computer Science and Electrical Engineering

CpE 271 Introduction to Logic Design - Syllabus
Spring 2015 – 3 Credit Hours

Instructor	Dr. Afzel Noore Room 949 ESB (Engineering Sciences Building) Phone: 304-293-9130 Email: afzel.noore@mail.wvu.edu
Office Hours	Tuesdays 2:00 pm to 3:00 pm Thursdays 2:00 pm to 3:00 pm
Class Time	12:30 pm to 1:45 pm
Class Location	Room 101 NRCCE (National Research Center for Coal and Energy)
Prerequisites	MATH 156
Textbook	Fundamentals of Logic Design by Charles H. Roth, 6th Edition Recommended – not required
Course Description	An introduction to the design of digital networks and computers. Topics include - number systems, coding, Boolean and switching algebra, logic design, minimization of logic, multiplexers, decoders, PLAs, sequential circuits, and design of digital subsystems.
Learning Outcomes	At the end of this course, a student should be able to: • Perform number base conversions and binary arithmetic • Evaluate logic functions • Minimize logic expressions using Boolean algebra and KMap • Design and analyze SSI/MSI/LSI Combinational Logic circuits • Design and analyze Synchronous Sequential circuits
Grading	Semester grades will be computed as follows: Exam 1 closed book/notes 25% Exam 2 closed book/notes 25% Exam 3 closed book/notes 25% Final Exam closed book/notes 25% (Comprehensive)
Semester Grade	$90 \leq A \leq 100$ $80 \leq B < 90$ $70 \leq C < 80$ $60 \leq D < 70$ $F < 60$

Class Policy

- ✓ General: You are expected to attend the class lectures. If you miss a class, you are responsible for all assignments and material covered. You are required to participate in all class discussions. You will be required to answer questions or discuss your solutions in class. The textbook is not required but can be used as a reference. You must maintain good class notes and should review all past materials covered before attending a class.

- ✓ Homework Assignments: Problems will be assigned in class to test your understanding of the material covered in class and immediate feedback will be provided to the whole class. These exercises are to help you determine your level of mastery of fundamental knowledge presented in class.

- ✓ Exams: Exams are designed to test your application of the knowledge learned. The questions will be more complex. All exams are closed book and closed notes. The final exam is comprehensive.

- ✓ Exam Dates: The dates for exams shown in the syllabus are tentative. They will be finalized in class. In case you miss a class, make sure you stay in touch with important announcements. Exams are given outside class hours on Thursday evenings.

- ✓ Make-up Exam: As a general policy, make-up exams will not be given. If there is an extenuating circumstance, you must contact your instructor before the exam and seek approval for granting a make-up exam. Usually the make-up will be a comprehensive exam to accommodate all students.

- ✓ Help in Learning: If you attended the lectures and did not understand the material, see your instructor before the next lecture. If you did not attend the class, first obtain the notes from your classmates, review the material, and then promptly see your instructor.

- ✓ Class Learning Environment: Cell phones must be turned off during class. Do not be late to class. Do not talk in class or read newspapers or do homework assignments from other classes. These activities disturb students and it is important to respect their right to a good learning environment in class.

- ✓ Plagiarism: Plagiarism will be severely penalized and may result in an F grade for the course or receive no credit for a specific exam. Students are expected to exhibit the same level of professionalism and integrity that will distinguish them in their professional careers. Both the student who copied the work and the student who allowed the work to be copied will be penalized. Consequences and procedures for dealing with cases of academic dishonesty are outlined in the WVU Student Code of Rights and Responsibilities.

- ✓ Students with Disability: If you have a disability and anticipate needing any type of accommodation in order to participate in this class, please advise your instructor and make appropriate arrangements with Disability Services (304-293-6700). The student should notify the instructor during the first week of class regarding the accommodation needed.

Tentative Lecture Schedule and Topics

Week 1 (January 13 and 15)

- Number Systems
- Number Base Conversions

Week 2 (January 20 and 22)

- Computer Codes
- Logic Gates

Week 3 (January 27 and 29)

- Logic Gates
- Evaluation of Switching Functions

Week 4 (February 3 and February 5)

- Analysis and Design of Combinational Logic Circuits
- Analysis and Design of Combinational Logic Circuits

Week 5 (February 10 and 12)

- Boolean Algebra
- **Exam 1 (7 pm, Thursday, February 12th)**

Week 6 (February 17 and 19)

- Boolean Algebra
- Simplification of Switching Functions using Karnaugh Maps

Week 7 (February 24 and 26)

- Simplification of Switching Functions using Karnaugh Maps
- Combinational Circuit Analysis using Multiplexers
  (FYI – Mid-semester – February 27th)

Week 8 (March 3 and March 5)

- Combinational Circuit Design using Multiplexers
- Combinational Circuit Analysis using Decoders

Week 9 (March 10 and 12)

- Combinational Circuit Design using Decoders
- Combinational Circuit Design using PLAs

Week 10 (March 17 and 19)

- Sequential Circuits
- **Exam 2 (7 pm, Thursday, March 19th)**
  (FYI – Last day to drop a class – March 20th)

Week 11 (March 21 through 29)

(FYI – No Class – Spring Recess)

Week 12 (March 31 and April 2)

- SR, D, JK, T Flip Flops
- Analysis of Sequential Circuits

Week 13 (April 7 and 9)

- Analysis of Sequential Circuits
- Analysis of Sequential Circuits

Week 14 (April 14 and 16)

- Design of Synchronous Sequential Circuits
- Design of Synchronous Sequential Circuits

Week 15 (April 21 and 23)

- Design of Synchronous Sequential Circuits
- **Exam 3 (7 pm, Thursday, April 23rd)**

Week 16 (April 28 and April 30)

- Digital Logic Design Examples
- Review
  (FYI – Last day to withdraw from University – April 30th)

Final Exam (Friday, May 8, 2015)

7:00 pm to 9:00 pm
Comprehensive Exam