Dr. Afzel Noore  
Room 949 Engineering Sciences Bldg  
304-293-9130  
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Monday  2:30 pm to 3:30 pm  
Wednesday  2:30 pm to 3:30 pm

Room 501 ESB

CPE 271 or equivalent, Graduate standing

- Class Notes  
- Use any textbook on Logic Design to supplement class notes  
- Journal Papers

Study of advanced combinational and sequential switching circuits, fault modeling in programmable logic array and complex CMOS gates, logic design using genetic algorithm.

At the end of this course, a student should be able to:

- Apply switching theory to the solution of logic design problems  
- Understand the complexities of design and testing with new technologies  
- Use evolutionary approach to switching circuit design

Semester grades will be computed as follows:

Exam 1  25%  
Exam 2  25%  
Project 1  25%  
Project 2  25%

90 ≤ A ≤ 100  
80 ≤ B < 90  
70 ≤ C < 80  
60 ≤ D < 70  
F < 60
Class Policy

General: Attendance at lecture is expected. If you miss a class, you are responsible for all assignments and material covered. You are required to participate in all class discussions. You will be required to answer questions or discuss your solutions in class. You must maintain good class notes and should review past materials covered before attending a class.

Homework: There will be no credits for homework assignments. Typically problems will be assigned in class. These exercises are to help you determine your level of mastery of knowledge presented in class.

Exams: Exams are designed to test your application of the knowledge learned. The problems in the exams is to make you think and will be extensions of problems solved in class. The exams will be closed-book. The projects will require performing literature search on research topics, understanding technical papers, and exploring new solutions.

Exam Dates: Dates for exams are tentative. They will be finalized in class. In case you miss a class, make sure you stay in touch with important announcements.

Missed Exam: As a general policy, make-up exams will not be given. If there is an extenuating circumstance, you must contact the instructor before the exam and seek approval for granting a make-up exam.

Help session: If you attended the lectures and did not understand any material, see the instructor promptly – before the next lecture. If you did not attend the class, first obtain the notes from your classmates, review the material, and then see your instructor for further clarification.

Plagiarism: Plagiarism will be severely penalized and may result in an F grade for the course or you may receive no credit for the specific exam or project. Students are expected to exhibit the same level of professionalism and integrity that will distinguish them in their future careers. Both the person who reproduced in whole or in any part from the work of others and the person who allowed the work to be copied will be penalized. Consequences and procedures for dealing with cases of academic dishonesty are outlined in the WVU Student Code of Rights and Responsibilities.

Disability: If you are a person with a disability and anticipate needing any type of accommodation in order to participate in this class, please advise me and make appropriate arrangements with the Office of Accessibility (Disability) Services (304-293-6700). For more information on West Virginia University's Diversity, Equity, and Inclusion initiatives, please see http://diversity.wvu.edu
Tentative Lecture Schedule and Topics

Week 1 (August 18th and 20th)
- Introduction to Logic Circuits
- Combinational Logic

Week 2 (August 25th and 27th)
- Minimization of Logic Functions
- Boolean Algebra

Week 3 (September 1st and 3rd)
- Boolean Algebra
  (FYI - Labor Day Recess, September 1st)

Week 4 (September 8th and 10th)
- Karnaugh Map
- Gate Transformation

Week 5 (September 15th and 17th)
- Multiplexer - Analysis
- Multiplexer - Design
- Project 1 – Background Demo Due

Week 6 (September 22nd and 24th)
- Decoder - Analysis
- Decoder - Design

Week 7 (September 29th and October 1st)
- Design with Programmable Logic Devices
- Design of Combinational Logic Circuits
  (FYI – October 3rd Mid-Semester)

Week 8 (October 6th and 8th)
- Design for testability of Programmable Logic Arrays
- Exam 1 (Outside class from 6:00 pm to 9:00 pm)

Week 9 (October 13th and 15th)
- Sequential Logic Circuits
  (FYI – October 13th and October 14th Fall Break Recess)

Week 10 (October 20th and 22nd)
- Project 1 – Demo (Outside class from 6:00 pm to 9:00 pm)
- Project 1 – Demo (Outside class from 6:00 pm to 9:00 pm)
  (FYI – Last Day to Drop a Class, Friday October 24th)
Week 11 (October 27th and 29th)
- Project 1- Report Due
- Analysis of Sequential Circuits
- Analysis of Sequential Circuits

Week 12 (November 3rd and 5th)
- Design of Synchronous Sequential Circuits
- Design of Synchronous Sequential Circuits

Week 13 (November 10th and 12th)
- CMOS Switching Logic Design

Week 14 (November 17th to 19th)
- CMOS Logic Testing
- Exam 2 (Outside class from 6:00 pm to 9:00 pm)

November 24th and 28th
(FYI - Thanksgiving Recess)

Week 15 (December 1st and 3rd)
- Project 2 Demo (Outside class from 6:00 pm to 9:00 pm)
- Project 2 Demo (Outside class from 6:00 pm to 9:00 pm)

Week 16 (December 8th)
- Project 2 - Report Due

(FYI – Last Day to Withdraw from the University, Monday Dec 8th)
(FYI – Last Day of Classes, Tuesday, December 9th)
(FYI – Wednesday, December 10th – Prep Day for Finals - Recess)
(FYI – Finals Week, Thursday Dec 11th through Wed Dec 17th)