The Lane Department of Computer Science and Electrical Engineering

EE 455: Introduction to Microfabrication

Semester: Fall 2014

Instructor: Xian-An Cao, Associate Professor
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Text: Fabrication Engineering at the Micro and Nanoscale, S. Campbell, Oxford, 4th edition, 2013.
Supplemental Material: lecture notes (on the course webpage)

Web Page: eCampus > Course Content
Assignments and solutions will be posted on the class web page. Time critical info will be sent to your MIX e-mail account.

Time/Location: Lecture, Tuesday and Thursday, 2:00-3:15pm, MRB 109
Office Hours: W/F 2-3 pm

Prerequisites: EE 355 (Analog Electronics), Semiconductor Physics or equivalent.

Course description: The continual evolution of integrated circuit fabrication technology over the last sixty years has resulted in today's Very-Large-Scale-Integrated (VLSI) circuits with billions of transistors per silicon chip. The fabrication technology has not only been refined to achieve nanoscale silicon devices on chips but also been used to transform present-day printed circuit boards into processed circuit wafers. This course will cover the fundamental micro- and nano- fabrication topics, including lithography, oxidation, diffusion, implantation, thermal processing, etching, thin film deposition, and metallization, as well as integrated fabrication processes central to silicon CMOS technologies. Broad applications of these processing techniques to the fabrication of other electronic and photonic devices will also be described.

Learning Outcomes: Students will develop a basic understanding of the physical mechanisms underlying unit and integrated micro-/nano-fabrication processes, an awareness of their capabilities and limitations, as well as hands-on experience in key processing techniques and equipment.

Tentative lecture schedule:

Major lecture and lab topics to be covered:	Approx. Week:
Technology Overview	1
Bulk crystals/wafers	2
Lithography	3,4
Quiz #1	
Diffusion	5
Oxidation	6,7
Ion Implantation/thermal processing	7,8
Simulation project assignment	
Cleanroom tour and demo	9
Midterm Exam	10
Etching	11
Physical Deposition	12
Quiz #2	
Chemical Deposition	13
Metallization and Interconnect	14
Integrated CMOS Process	16
Final Exam	

EE 455 COURSE RULES AND OPERATIONAL GUIDELINES

1) *General:* Due to the current nature of much of the subject matter, lectures will provide the nucleus of the material covered in this class. Selected sections in the textbook may be assigned to supplement and expand upon lectures. Handouts, verbal instructions and demonstrations may not always be scheduled in advance but will occur when appropriate for the topic. Attendance is required. Students missing a class are responsible for all material covered.

2) *Exams &Grades:* Semester grades will be computed roughly as follows:

Homework	10%
Quizzes 1 & 2	10%
Cleanroom tour and demo	5%
Process simulation project	15%
Midterm Exam	25%
Final Exam	35%

Tests will seek to determine your level of mastery of fundamental principles and methods developed in the lectures and text and reinforced/expanded upon through homework assignments. Grades will generally be 90-100% =A, 80-89% =B, 70-79% =C, etc. The approximate test dates and project due are:

Midterm: Week 10
Final Exam: final week
Simulation project report: due 12/09/14

The actual exam dates will be chosen during class. Consistent with WVU guidelines, students absent from regularly scheduled exams because of authorized university activities will have the opportunity to take them at an alternate time. Make-up exams for absences due to any other reason will be at the discretion of the instructor.

3) *Homework and reports:* There will be 5-6 homework assignments given throughout the semester. Homework is due at the start of class on the due date. Each set of homework will be given a letter grade. The report of the process simulation project will account for 15% of the final grade. Unexcused late homework and report will lose points. Solutions will be provided for all problems and problems of particular interest will be reviewed in class. Students are encouraged to conceptually discuss homework and project assignments but must submit their own independent assignments. If you do not fully understand homework, text, and lecture material, see me promptly.

4) *Academic Integrity:* The integrity of the classes offered by any academic institution solidifies the foundation of its mission and cannot be sacrificed to expediency, ignorance, or blatant fraud. Therefore, I will enforce rigorous standards of academic integrity in all aspects and assignments of this course. For the detailed policy of WVU regarding the definitions of acts considered to fall under academic dishonesty and possible ensuing sanctions, please see the Student Conduct Code at http://www.arc.wvu.edu/admissions/integrity.html. Should you have any questions about possibly improper research citations or references, or any other activity that may be interpreted as an attempt at academic dishonesty, please see me before the assignment is due to discuss the matter.

WVU Social Justice Statement:

The West Virginia University community is committed to creating and fostering a positive learning and working environment based on open communication, mutual respect, and inclusion. If you are a person with a disability and anticipate needing any type of accommodation in order to participate in this class, please advise me and make appropriate arrangements with the Accessibility Services (293-6700). For more information on West Virginia University's Diversity, Equity, and Inclusion initiatives, please see http://diversity.wvu.edu.