Course Syllabus

CpE 442/ CS 455

INTRODUCTION TO COMPUTER ARCHITECTURE

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Office Hours: Tuesdays- Thursdays: 11:00 -12:00,
Mondays - Wednesdays 3 – 4 pm with appointments.

Prerequisites: CPE 271


References:

COURSE OBJECTIVES:

Students should be able to do the following:

- Relate performance metrics to architectural parameters.
- Specify the important tradeoffs in instruction set design.
- Identify the problems and tradeoffs encountered in the design of computer processors, and specify specific example from the current state of the art family of Reduced Instruction Set Architectures (the MIPS architecture).
- Relate the concept of memory hierarchy to cache designs and the design of virtual memory management units.
- Identify the problems encountered in I/O subsystem design, and relate such problems to the design of processor and memory subsystems, and identify new technologies for disks and tapes.
- Identify the main features of parallel architectures in terms of interconnection networks and the extended concepts of instruction set parallelism

**Topics:**

<table>
<thead>
<tr>
<th>Topic</th>
<th>#weeks</th>
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<tr>
<td>Overview of Computer Architecture</td>
<td>Ch. 1.1-1.3, 1/2</td>
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<td>The Role of Performance</td>
<td>Ch. 1.6, 1.9 1</td>
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<td>Instruction Set Design Tradeoffs</td>
<td>Ch. 2 1</td>
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<td>The MIPS Instruction Set Architecture</td>
<td>Ch 2 1</td>
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<td><strong>The Processor Data Path and Control</strong></td>
<td>Ch 4.1-4.4 3</td>
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<td>The Single Cycle Data Path</td>
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<td>The Single Cycle Control</td>
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<td>The Multi Cycle Data Path</td>
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The Multi Cycle Control,
Microprogramming and Exceptions

- **Pipelining Architecture**  Ch 4.5 - 4.9  2
  Design of a Pipeline Processor I
  Design of a Pipeline Processor II

- **The Memory Hierarchy**,  Ch 5  2
  The Memory Subsystem
  Cache Design
  Virtual Memory

- **I/O Characteristics and Performance**,  1
  The I/O Subsystem
  Bus Architectures

- **Introduction to Parallel Architectures**,  1/2
  Interconnection Networks
  Instruction Level Parallelism

- **Review for the term exam**  1

- **Project Presentations: Last two Weeks of Classes**, See Term Project Assignment  2

**Grading:**

- Attendance  10%
- Assignments  25%
- Project  35%  here is an example previous presentation and report

Project Presentations held during the last 2 weeks of classes
Project Report due Thursday of Finals Week
Term Examination  30%, Tentative Date: in Class Exam. The Thursday Before Thanksgiving Break

The project involves a comprehensive study of a processor architecture. The overview of the architecture and how it briefly compares to others and details of some of its main features should be thoroughly researched. The projects will be conducted by groups of 3-4 students. A final report and an in-class presentation are required. The report should contain a section on the contributions of each member of the group, and each member should take part in the project presentation.