AREA 3 - COMPUTER SYSTEMS

Core Courses

CpE 670	Switching Circuit Theory
CS 550	Theory of Operating Systems

Approved Faculty Examiners

CpE 670	Dr. Powsiri Klinkhachorn
	Dr. Afzel Noore
CS 550	Dr. Vinod Kulathumani
	Dr. Jim Mooney

PhD Qualifying Exam Topics

CpE 670 Switching Circuit Theory

COMBINATIONAL LOGIC

1. Analysis
2. Design

MINIMIZATION OF LOGIC FUNCTIONS

1. Boolean algebra
2. K-Maps

MULTIPLEXERS, DECODERS, and PLAS

1. Analysis
2. Design

SEQUENTIAL LOGIC

1. Analysis
2. Design

REFERENCES

1. Any logic design text book
2. Class notes

CS 550 Theory of Operating Systems

CONCURRENCY

1. The mutual exclusion problem
2. Semaphores
3. Monitors
4. General synchronization issues
5. Deadlock

SCHEDULING

1. Scheduling objectives and criteria
2. Batch and interactive algorithms
3. M/M/1 queueing models
4. Interactive models and saturation point

MEMORY MANAGEMENT

1. Paging concepts
2. Page replacement algorithms
3. Global vs. Local replacement
4. Cost measures
5. Inclusion Property

DISTRIBUTED SYSTEMS

1. General design issues
2. Event ordering and its applications
3. Handling deadlock
4. Atomic transactions and stable storage
5. Distributed file system design

REALTIME SYSTEMS

1. General design issues
2. Hard vs. Soft realtime
3. Rate-Monotonic scheduling and theorem
4. Dynamic scheduling

REFERENCES

1. Silberschatz, Galvin and Gagne, *Operating System Concept*s, 8th Edition, John Wiley & Sons, 2009, Chapters 5-7, 9, 16-19
2. Allen, A. O. *Queueing Models of Computer Systems*, IEEE Computer, Vol. 13, No. 4, April, 1980, pp. 13-24.