CpE-310 Microprocessor Systems

[Jan 2, 2015]

Semester : Spring 2015
Home page: ecampus.wvu.edu

Location: G 83
Time 13:00-13:50 MWF

Course Format
and Credit Hours : 3 hr Lecture, 3 hr Credit

Instructor : Yaser P. Fallah
Office: 831 ESB
Tel: 304-293-1660
e-mail: Yaser.fallah@mail.wvu.edu
Office Hours: 2:00pm MWF right after class is a good time. For other times, feel free to stop by or by appointment, but please call or e-mail to be sure I will be in my office. If you are outside the building, call first to be sure I will be in and available when you arrive.

Required Texts: 1. The INTEL Microprocessor Family: hardware and software principles and applications
By James L.Antonakos, Thomson, ISBN 1-418-03845-8
OR Third Edition is fine as well (ISBN = 0-13-893439-8

Pre-requisites : CpE-271
Co-requisites : CpE-311

[*Recommended* PR: CpE-272, EE-251, and EE-252, (and by default EE-221 and EE-222, Physics, and Math 156. If you are an EE or a CpE and have not completed EE-251 and EE-252, you may have serious trouble with labs in this course! CS students get a waiver on this.]

Course Objectives: To present the theory and design of microprocessor systems; organization and architecture of modern processors; integration of microprocessors with RAM, ROM, and I/O devices; machine language, assembly language, and software development.

Expected Learning Objectives:
Upon successful completion of this course:

1. Architecture: the student shall be able to:
    a) draw an overall computer architecture diagram
    b) draw a detailed architecture diagram of the INTEL-8086.
    c) design an address decoder
    d) draw block address decoder
    e) describe two major types of memory
    f) describe the three major types of input output
    g) draw disk drive, tracks, sectors, and cylinders
    h) draw the Interrupt process flow
    i) draw a PC diagram using north bridge, south bridge and all attached busses.
2. Assembly Language: the student shall be able to:
    a) write a program in assembly language for the INTEL 80x86
    b) hand assemble assembly code to machine code.
    c) use all addressing modes in assembly language.
3. I/O Interfacing: the student shall be able to:
    a) draw a design for an output port I/F to light an LED
    b) draw a design for input port I/F to read a switch position
4. Digital Communications: The student shall be able to:
    a) draw an Asynchronous data transmission timing diagram
    b) interface an RS-232 device
    c) draw a time and/or frequency domain diagram for standard modems

Grading : Semester grades for CpE 310 will be computed as follows:

Homework and quizzes:	30%
Attendance	5%
Examinations	
Mid-Term	30%
Final (COMPREHENSIVE)	35%
	100 %

Grade Assignment : A= 90-100
B= 80-89
C= 70-79
D= 60-69
F= 59 and below

Grading Policy :

1. Late Homework: Late homework is not acceptable. Homework is due on e-Campus at the time it is due. Late homework will be worth zero.

2. Joint work: Students are encouraged to discuss homework

assignments but **must** submit their own individually prepared assignments. Jointly prepared and/or copied assignments **WILL** be severely penalized.

Notes on academic dishonesty :

- I consider it academic dishonesty if you share final assignments, work, solutions, etc with other students.
- Changing variable names and/or output messages on code does not make original work!
- If code is "reused," you must site the source and should cite it in the comments for that code or routine.
- Allowing others to view your work by leaving permissions set incorrectly or leaving files on hard drives or other disks accessible by others will be considered academic dishonesty (not to mention poor security practice on your part.)
- IF a student does discuss and share work with another, thinking that the person who is receiving that information will not copy it, both people will be held responsible for academic dishonesty if identical work is submitted and both claim that it is original.

3. Makeup Exams: No make-up exams (except by prior arrangement with the instructor.)

HW Assignments: Homework assignments will be given periodically. Each assignment will be worth approximately the same amount of credit (Typically there will be five or more homework assignments and five or more quizzes. Each will be counted towards the final grade with a total worth 30 %). Assignments are due at the time and date assigned submitted on e-campus. No late HW or other assignments will be accepted.

HW Assignments e-Campus: All class communications will be via ecampus.wvu.edu which is accessed with your mix e-mail account name and password. Assignments will be posted on e-Campus. ALL ASSIGNMENTS will be submitted on e-campus. No paper copies will be accepted.

Attendance Policy: Attendance at all class sessions is REQUIRED. Attendance will be taken at some class sessions and will count 5 % of the final grade as shown above. Consistent with WVU guidelines, students absent from regularly scheduled examinations because of authorized University activities will have the opportunity to take them at an alternate time provided that arrangements are made before the test; homework for such activities shall be submitted before the absence occurs. Make-up exams for absences due to any other reason will be at the discretion of the instructor and will not generally be granted.

QUIZES: Quizzes may be given with no notice.

Class distractions: Cell phones, pagers, etc must be turned OFF during class. These are distracting for all. Headphones are prohibited.

Laptops in Class: You may use your laptop in class provided that you are using it to take notes or to view class related pages for class notes. E-mail, IM, general surfing and game playing are forbidden!! Headphones are also strictly prohibited.

Course Schedule

TOPICS

A) Computer Architectures
   1) Basic physical architecture of microprocessor (notes).
      Overall Architecture types (Harvard Vs Von Neumann)
      Overall Architecture Diagrams
      Single bus vs Multiple bus architectures
      Chap 1
      [You must be able to draw a general architecture diagram.]
   2) Registers (8086 16 bit-example), Why use
      Address & Data Registers
   3) Special Purpose Registers, Why do we need
      Program Counter
      Status Register
   4) Memory, Introduction to
      RAM, how addressing works, Post Office example
   5) Simple Instruction examples (for the 8086)
      MOVE, ADD, NOP, JMP
   6) Addressing modes (example 80x86)
      Immediate
      Absolute
      Register
         Direct
         Indirect
      PC-relative
      more…..
   7) Branching
      JMP unconditional
      Jump conditional
      Loop
      Stack Pointer and Stack allocation
   8) Jump subroutine (JSR)
   9) Memory

1) RAM, ROM, PROM, EPROM, UVEPROM, EEPROM
2) Static random access memory (SRAM)
3) Dynamic random access memory (DRAM)
4) Addressing
    Byte Addressing
    Word Addressing
    Long Word Addressing

10) Instruction formats
    Program Control hardware
    Program Counter
    Instruction Format options
    Multiple word instructions
    Assembly language vs machine code
    Flag Register
    Segment Registers
        Real Mode
        Protected Mode

[You must be able to draw an 8086 architecture diagram including detail of all registers and data paths]

[You MUST be able to:]
[1. Write a program in Assembly Language]
[2. Hand assemble to machine code]
[3. Use all addressing modes]
[4. Hand operate the machine cycle by cycle]

B) Microprocessor Hardware
2) Pin Definitions
3) Clock rates

C) Parallel Input/Output
1) General Parallel I/O
2) Address decoding (Page 407)

[You must be able to design an address decoder]

3) Parallel Interface/Timer Chips,
    Modes of operation
    Double Buffering
    Output register
    Output port Registers and addressing

D) Microprocessor Bus
1) Internal Vs External Buses
2) Addressing
3) Memory maps (example lab board)
4) Full Address Decode Vs Block Address Decode

[You must be able to draw Block Address Decoding]

5) Asynchronous Vs synchronous Bus
6) PC buses
    ISA (8Mhz)
    EISA
    VESA
    PCI (33 MHz)
    AGP
    USB
7) North Bridge, South Bridge.

[You must be able to draw a PC diagram showing all buses, bridges and speeds.]

E) Secondary Memories
1) Disk Drives
    Track, sector, cylinder,
    Disk Drives, Hard drive, CD Drive, DVD

[You must be able to draw disk drive, tracks, sectors, and cylinders]

2) Cache memory
    L1 and L2

F) Peripheral Interfacing
1) Drivers (Review of Open collector, Tri-state, etc)
2) Driving LED's, How to
3) Reading Switches, How to
4) A/D and D/A converters

[You must be able to draw a design for an output port I/F to light an LED.]
[You must be able to draw a design for input port I/F to read a switch position.]

G) I/O Programming
1) Programmed I/O
2) Interrupts and interrupt programming
    Interrupt request, Interrupt Priority, Interrupt Mask
3) DMA, Direct Memory Access

[You must know the three major types of I/O.]
[You must be able to draw the Interrupt process flow.]

H) Serial Input/Output
1) RS-232 serial ports
2) UARTs and DUARTs
4) RS-422, RS-423

[You must be able to draw an Asynchronous RS-232 data transmission timing diagram.]
[You must know how to interface an RS-232 device.]

I) Digital Communications
1) Modems
    ASK, FSK, PSK, QSK, Cable modem, ADSL, POTS
2) OSI/ISO levels

3) Physical Layer
Ethernet, 10-base-T, 100-base-T, ATM

[You must be able to draw a time and/or frequency domain diagram for STD modems.]
[You must be able to draw and explain a typical TCP/IP packet.]
[You must be able to calculate the value of a subnet mask.]

J) Advanced Topics: (Time permitting, basic concepts, less heavily treated than in textbooks. Topics may differ from those listed below.)

1) Basics of memory management and virtual memory (parts of sections 7.2 and notes). 2
2) Cache memory techniques . 1
3) Basics of math coprocessors 1
4) CRT Displays 1
5) Multiprocessing

Course Goals :

In CpE-310, the student will develop a working understanding of contemporary 16/32-bit microprocessors (using the INTEL 80x86family of microprocessors as examples) and their expanding role as software-controlled elements of digital systems (embedded computers.) The companion laboratory (CpE-311) will use a commercial 80x86 based single board computer (SBC) made by Octagon systems Inc. to help students gain practical experience with both programming (assembly language) and interfacing to applications.

Lectures in CpE-310 will emphasize the underlying principles associated with microprocessors, starting with the programmer's model and the general internal architecture of microprocessors. Assembly language programming, providing an understanding of the fundamental microprocessor instruction sets and addressing modes, will be presented, providing the student with an appreciation of the low-level structure of executable programs supported by lab projects using the laboratory single board computer. Lectures will then extend to other hardware issues, including execution times, microprocessor buses, memory hardware, I/O functions such as serial and parallel ports and an introduction to modem communications protocols. Interfacing of special purpose peripherals to a microprocessor is discussed, leading to a final project in the laboratory, CpE-311. Advanced topics including digital communications, cache memory, memory management, while such things as floating point coprocessors will be discussed if time permits.

West Virginia University is committed to social justice. I concur with that commitment and expect to maintain a positive learning environment based upon open communication, mutual respect, and non-discrimination. Our University does not discriminate on the basis of race, sex, age, disability, veteran status, religion, sexual orientation, color or national origin. Any suggestions as to how to further such a positive and open environment in this class will be appreciated and given serious consideration.

If you are a person with a disability and anticipate needing any type of accommodation in order to participate in this class, please advise me and make appropriate arrangements with Disability Services (293-6700).

ACADEMIC DISHONESTY POLICY

As a student in the Lane Department of Computer Science and Electrical Engineering, you are expected to behave ethically and professionally. In addition to the WVU policies on cheating in the WVU student Handbook, **http://www.arc.wvu.edu/rightsa.html** the Lane Department and your instructor add the following.

In particular, academic dishonesty, including plagiarism and cheating, will not be tolerated.

If you submit any assignment -- report, project, homework, portfolio, exam, etc. -- under your name that has been reproduced in any part or in whole from the work (paper or electronic) of others without specifically citing the source, you are being academically dishonest. You are also being dishonest if you knowingly allow your work to be submitted by someone else without acknowledgement that it is yours.

If you are found to be academically dishonest, in addition to WVU sanctions that can lead to expulsion from the program, and/or from WVU, the Lane Department and the Professor will take the following action:

Per the Student Handbook, the instructor may choose any of the following:

- -- you may receive a zero score for the applicable assignment. A notation will be placed in your student file (if you are a Lane Department major) AND sent to your advisor and the Department Chair.
- – you may receive an "unforgivable F" in the applicable course.
- – you may be dismissed from the class and prevented from taking any Lane Department class in the future.
- -- you may be dismissed from WVU.

These actions may be appealed following the process outlined in the WVU Student Code of Rights and Responsibilities.

Additionally, a letter will be put in your student file. You should know it may affect future internship, work, or job opportunities.