COURSE SYLLABUS

CPE 442/ CS 455
Introduction to Digital Computer Architecture

Course Introduction

Credit Hours: 3
Prerequisite Courses: MATH 375 or MATH 378 and CPE 310 or CPE 320
Instructor: Mohamed Hefeida, PhD, Teaching Associate Professor
Class Meets: TR 9:30 - 10:45 / Online; Aug 26 - Dec 10
Class Meeting Zoom Link (Registration Required):
https://wvu.zoom.us/meeting/register/tJcldO6rqz0pEtzAjYQFeLiaJDd6S4XVe3DF

Course Introduction:
This course introduces high-performance computer architecture in a systemic manner. First, it
discusses two fundamental design parameters: instruction set architecture (ISA) and
performance evaluation. Then, it introduces dynamically scheduled superscalar techniques,
including multi-issue, dynamic instruction scheduling, speculative execution, branch prediction,
memory dependence speculation, and instruction level parallelism (ILP). Next, advanced cache
designs, including multi-level cache, high-performance instruction cache, multi-port data cache,
and other techniques will be studied. Those techniques address the performance loss from the
increasing CPU-memory speed gap. Finally, the main features of parallel architectures in
terms of interconnection networks and the extended concepts of instruction set parallelism will
be discussed.

Faculty Contact Information

Instructor Office Location: AER 255
Office Hours: T: 11-12 and R: 2-3
Office Hours Zoom Link: https://wvu.zoom.us/j/93105418665
Instructor Email and/or Phone: msh00015@mix.wvu.edu / (304) 293-4326

Instructional Materials

Required Instructional Materials:
Hennessy and D. A. Patterson, Morgan Kaufmann Publishers, Inc.
Technology Requirements: Broadband Internet Connection, Computer, WebCam, microphone, and Scanner

Software: Open Source

Website: eCampus

Optional Instructional Materials:
IEEE/ACM Libraries, and other scientific journals/magazines

Course Learning Outcomes

Course Learning Outcomes:
- Relate performance metrics to architectural parameters.
- Specify the important tradeoffs in instruction set design.
- Identify challenges and tradeoffs encountered in the design of processors.
- Relate the concept of memory hierarchy to cache designs and memory management units.
- Identify the problems encountered in I/O subsystem design, and relating them to the design of processor and memory subsystems.
- Identify the main features of parallel architectures in terms of interconnection networks and the extended concepts of instruction set parallelism.

Assessment

Short Descriptions of and Grading Criteria for Major Assignments/Assessments:
1- Quizzes (60%): There will be a quiz approximately every Thursday, each quiz is worth 10%. Only the best 6 grades will count towards your final grade. Quizzes will be based on hw assignments and/or lecture content.

2- Project (15%): Report, and presentation.

3- Term Exam (25%): Comprehensive Term Exam

Weight/Distribution of Course Points:
Quizzes (60%); Project (15%); Exam (25%)

Mid-Semester Grade:
2 Quizzes: 2X10%=20%
Expected Timeline of Major Assignments/Assessments and Topics/Units:
Weekly Quizzes

Final Grading Scale:
A: 90 - 100; B: 80 – 89; C: 70 – 79; D: 60-69; F:≤59

Course and Institutional Policies

Attendance Policy:
You must attend classes in order to be able to take the weekly quizzes (every Thursday). These quizzes are worth 50% or your final grade and you will not be able to pass the course without attending these classes/quizzes. No late assignments or makeups will be allowed for any assessment.

Participation Policy:
I encourage sharing thoughts; however, I consider it academic dishonesty if you share assignment/exam solutions. Grades assigned during the semester on exams, quizzes, reports, or homework assignments are considered final after one week of grading/getting back your assignment. Common standards of academic integrity prohibit not only cheating or plagiarizing, but also the unethical conduct of trying to obtain grades that the student has not earned. Violations of academic integrity are described in the WVU Catalog: http://bit.ly/2hDAeUa.

The West Virginia University community is committed to creating and fostering a positive learning and working environment based on open communication, mutual respect, and inclusion. If you are a person with a disability and anticipate needing any type of accommodation in order to participate in this class, please advise me and make appropriate arrangements with the Office of Disability Services (293-6700). For more information on West Virginia University’s Diversity, Equity, and Inclusion initiatives, please see http://diversity.wvu.edu.

Late Assignment and Missed Exam Policy:
No late assignments or makeups will be allowed.

Institutional Policies:
Students are responsible for reviewing policies on inclusivity, academic integrity, incompletes, sale of course materials, sexual misconduct, adverse weather, as well as student evaluation of instruction, and days of special concern/religious holiday statements.