The Lane Department of Computer Science and Electrical Engineering

EE 455: Introduction to Microfabrication

Semester: Fall 2019

Instructor: Prof. Xian Cao
AERB 346, Email: xacao@mix.wvu.edu

Text: Fabrication Engineering at the Micro and Nanoscale, S. Campbell, Oxford, 4th ed., 2013.
Supplemental Material: lecture notes

Web Page: eCampus - Assignments and solutions will be posted on the course webpage. Time critical info will be sent to your MIX e-mail account.

Time/Location: Lecture, Tuesday and Thursday, 12:30-1:45pm, ESB 449
Office Hours: T/R 11-12 pm

Prerequisites: EE 355 (Analog Electronics), Semiconductor Physics or equivalent.

Course description: The continual evolution of integrated circuit fabrication technology over the last sixty years has resulted in today's Ultra-Large-Scale-Integrated (ULSI) circuits with billions of transistors per silicon chip. The fabrication technology has not only been refined to achieve nanoscale silicon devices but also been used to transform circuit design blueprints into processed microchips. This course covers the fundamental micro- and nano- fabrication topics, including lithography, etching, implantation, oxidation, thermal processing, thin film deposition, and metallization, as well as integrated fabrication processes central to the silicon CMOS technology. Broad applications of these processing techniques to the fabrication of other electronic and photonic devices will also be described.

Learning Outcomes: Students will develop a basic understanding of the physical mechanisms underlying unit and integrated micro-/nano-fabrication processes, an awareness of their capabilities and limitations, as well as the development trend of electronic manufacturing technologies.

Tentative lecture schedule:

Major lecture and lab topics to be covered:	Approx. Week:
Technology Overview	1
Semiconductor Substrates	2
Lithography	3,4
Etching	5
Test #1	
Ion Implantation/Thermal Processing	6,7
Oxidation	8,9
Test #2	
Process simulation project	
Physical Deposition	10
Chemical Deposition	11
Test #3	
Metallization and Interconnect	12,13
Integrated CMOS Process	14-16
Final Exam	

EE 455 COURSE RULES AND OPERATIONAL GUIDELINES

1) *General:* Due to the current nature of much of the subject matter, lectures will provide the nucleus of the material covered in this class. Selected sections in the textbook may be assigned to supplement and expand upon lectures. Handouts, verbal instructions and demonstrations may not always be scheduled in advance but will occur when appropriate for the topic. Attendance is strongly encouraged. Students missing a class are responsible for all the material covered which may not be found in the textbook.

2) *Exams &Grades:* Semester grades will be computed roughly as follows:

Tests 1-3	20%×3 = 60%
Final Exam	25%
Process simulation	15%

Tests will seek to determine your level of mastery of fundamental principles and methods developed in the lectures and text and reinforced/expanded upon through homework assignments. Grades will generally be 85-100% =A/A-, 75-84% =B, 65-74% =C, etc. The actual test dates will be chosen during class. Consistent with WVU guidelines, students absent from regularly scheduled exams because of authorized university activities will have the opportunity to take them at an alternate time. Make-up exams for absences due to any other reason will be at the discretion of the instructor.

3) *Homework and reports:* There will be about 6 homework assignments given throughout the semester. Solutions will be provided for all problems and problems of particular interest will be reviewed in class. The report of the process simulation project will be due around Week 14. Unexcused late report will lose points. Students are encouraged to conceptually discuss homework and project assignments but must submit their own original work. If you do not fully understand homework, text, and lecture material, email or see me promptly.

4) *Academic Integrity:* The integrity of the classes offered by any academic institution solidifies the foundation of its mission and cannot be sacrificed to expediency, ignorance, or blatant fraud. It is important for you to maintain the highest ethical standards as outlined in WVU's Student Conduct Code and Discipline Procedure, which can be found online at http://bit.ly/2hBUt4P. I will enforce rigorous standards of academic integrity in all aspects and assignments of this course. The definitions of acts considered to fall under academic dishonesty and possible academic penalties are described in WVU Catalog: http://bit.ly/2hDAeUa. Should you have any questions about possibly improper research citations or references, or any other activity that may be interpreted as an attempt at academic dishonesty, please see me before the assignment is due to discuss the matter.

5) *Social Justice Statement:* The West Virginia University community is committed to creating and fostering a positive learning and working environment based on open communication, mutual respect, and inclusion. If you are a person with a disability and anticipate needing any type of accommodation in order to participate in this class, please advise me and make appropriate arrangements with the Accessibility Services (293-6700). For more information on West Virginia University's Diversity, Equity, and Inclusion initiatives, please see http://diversity.wvu.edu.