

WEST VIRGINIA UNIVERSITY
COLLEGE OF ENGINEERING AND MINERAL RESOURCES
THE LANE DEPARTMENT OF COMPUTER SCIENCE AND
ELECTRICAL ENGINEERING

Course Syllabus

CpE 442/ CS 455

INTRODUCTION TO COMPUTER ARCHITECTURE

Instructor: Hany H. Ammar, Professor of Computer Engineering, Office: 246 AER, Evansdale Campus, WVU, Morgantown, WV 26506, Ph: 293-9682

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Office Hours: Tuesdays- Thursdays: 11:00 -12:00,

Mondays - Wednesdays 3 – 4 pm with appointments.

Prerequisites: CPE 271

Text: Computer Organization and Design: The Hardware/Software Interface, **MIPS Edition, 5th Ed.**, D. A. Patterson and J. L. Hennessy, Morgan Kaufmann Publishers, 2014.

https://www.amazon.com/Computer-Organization-Design-MIPS-Architecture/dp/0124077269/ref=sr_1_fkmr0_1?keywords=%3A+Computer+Organization+and+Design+%3A+The+Hardware%2FSoftware+Interface%2C+5th+Ed&qid=1566148263&s=books&sr=1-1-fkmr0

References:

1. Cloud Computing for Machine Learning and Cognitive Applications, by Kai Hwang, MIT Press, (June 16, 2017).
2. Structured Computer Organization, A. S. Tanenbaum, Prentice-Hall.
3. Computer Hardware/Software Architecture, W. Toy and B. Zee, Prentice-Hall.
4. Modern Computer Architecture, Mohammed Rafiguzzaman and R. Chandra, West Publishing Company.
5. Computer Organization, 5th ed, C. Hamacher, Z. Varbesic, S. Zaky, McGrawHill.

COURSE OBJECTIVES:

Students should be able to do the following:

- Relate performance metrics to architectural parameters.
- Specify the important tradeoffs in instruction set design.
- Identify the problems and tradeoffs encountered in the design of computer processors, and specify specific example from the current state of the art family of Reduced Instruction Set Architectures (the MIPS architecture).
- Relate the concept of memory hierarchy to cache designs and the design of virtual memory management units.
- Identify the problems encountered in I/O subsystem design, and relate such problems to the design of processor and memory subsystems, and identify new technologies for disks and tapes.
- Identify the main features of parallel architectures in terms of interconnection networks and the extended concepts of instruction set parallelism

Topics:

#weeks

- <u>Overview of Computer Architecture</u> Ch. 1.1-1.3,	1/2
- <u>The Role of Performance</u> , Ch. 1.6, 1.9	1
- <u>Instruction Set Design Tradeoffs</u> , Ch. 2	1
- <u>The MIPS Instruction Set Architecture</u> Ch 2	1
- The Processor Data Path and Control Ch 4.1-4.4	3
<u>The Single Cycle Data Path</u>	
<u>The Single Cycle Control</u>	
<u>The Multi Cycle Data Path</u>	

